UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,237	07/29/2003	Makoto Shizukuishi	107317-00060	4755

7590 11/30/2007

ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
Suite 400
1050 Connecticut Avenue, N.W.
Washington, DC 20036-5339

EXAMINER
TRAN, NHAN T

ART UNIT	PAPER NUMBER
2622	

MAIL DATE	DELIVERY MODE
11/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/628,237	SHIZUKUISHI, MAKOTO	
	Examiner	Art Unit	
	Nhan T. Tran	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed 11/13/2007, with respect to the rejection(s) of claim(s) 1-19 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of a new combination of Tran et al. and Morris et al. as set forth below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-8, 14-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tran et al. (US 6,282,145) in view of Morris et al. (US 6,573,936).

Regarding claim 1, Tran discloses a solid state image pickup device (integrated image pickup device shown in Fig. 1D) comprising:

a semiconductor substrate (2005) defining a two-dimensional surface (Fig. 1D and col. 6, lines 34-42);

a number of photoelectric conversion elements (inherent pixels of image sensor 2003) disposed in a light receiving area of said semiconductor substrate in a matrix

shape and in a first number of rows and a second number of columns (see Fig. 1D; col. 6, lines 34-46 and col. 1, lines 16-17, and it is noted that since the image sensor 2003 is a mega-pixel image sensor, the rows and columns of pixels are inherent);

an analog digital converter (A/D 2002 in Fig. 1D), formed in an area of said semiconductor substrate other than the light receiving area, said analog digital converter converting analog image data from said photoelectric conversion elements into digital image data (col. 6, lines 34-48);

a non-volatile memory (memory 2000 in Fig. 1D) formed in an area of said semiconductor substrate other than the light receiving area at a succeeding stage of said analog digital converter, said non-volatile memory having memory units (i.e., memory cell), each corresponding to one of the photoelectric conversion elements, and recording the digital image data (col. 6, lines 34-58 and col. 7, lines 11-13, wherein the image signals output from the photoelectric conversion elements are stored into the memory 2000 after A/D converting processing in raw uncompressed format that meets the limitations of "each corresponding to one of the photoelectric conversion elements").

Although Tran discloses the analog digital converter (A/D 2002), Tran does not explicitly disclose a plurality of A/D converters, each formed for each column of said photoelectric conversion elements.

However, Morris teaches an integrated image pickup device in which an A/D converter array (120) includes plurality of A/D converts, each corresponding to one column of pixels (102_n) in a parallel architecture (Fig. 1) for improving performance by parallel processing (see Morris, col. 2, lines 10-66).

Therefore, it would have been obvious to one of ordinary skill in the art to modify the image pickup device in Tran to provide an A/D converters array, each formed for each column of said photoelectric conversion elements so as to improve performance of the device by parallel processing of the signals output from the photoelectric conversion elements as taught by Morris.

Regarding claim 2, it is also clearly seen in Tran that the non-volatile memory records the digital image data of one frame (see Tran, col. 6, lines 34-58 and col. 7, lines 26-31 in which the non-volatile memory is a giga-bit high density memory that is fully capable of storing a full frame of image data).

Regarding claim 3, it is also clearly seen in Tran that the non-volatile memory records the digital image data of a plurality of frames (see Tran, col. 6, lines 34-58 and col. 7, lines 26-31 in which the non-volatile memory is a giga-bit high density memory that is fully capable of storing a plurality of frames).

Regarding claim 4, Tran in view of Morris further discloses erasing means for erasing the digital image data and transferring means for transferring image data to an external device (see Tran, col. 8, lines 45-50). Although Tran and Morris are silent as to erasing the digital image data after the digital image data stored in said non-volatile memory is read to an external device, it is easily recognized by one skilled in the art

from the teaching of Tran above to erase the image data after being transferred to an external device to provide memory space for subsequent images.

Therefore, it would have been obvious to one of ordinary skill in the art to reconfigure the device in Tran and Morris to erase the image data after being transferred to an external device to provide memory space for subsequent images.

Regarding claim 5, as disclosed by Tran in col. 7, lines 11-13 that the image pickup device stores uncompressed image data into the non-volatile memory 2000 without rotating (no automatic rotation of image is taught). Thus, the disclosure of Tran encompasses "addresses of said non-volatile memory in a vertical direction are related to addresses of the light receiving area in the vertical direction." since the memory 2000 stores original (raw) image data and its orientation.

Regarding claim 6, as shown in Fig. 1D of Tran, the micro-controller 2001 indicates a common data register for both data input and output for said non-volatile memory.

Regarding claim 7, Tran in view of Morris as discussed in claim 1 further discloses that said non-volatile memory has a depth of same bits (8 bits) as output bits of said analog digital converters provided for each column (see Tran, col. 14, lines 18-24 and Morris, col. 2, lines 56-58).

Regarding claim 8, Tran in view of Morris as discussed in claim 1 also teaches that each of said analog digital converters (120 in Morris) outputs the digital image data of one row of said photoelectric conversion elements in parallel, and said non-volatile memory records the digital image data of one row output parallel at a memory position corresponding to a row direction (see Morris, col. 2, lines 54-66 and Tran, col. 14, lines 18-24).

Regarding claims 14 & 15, as clearly disclosed by Tran in col. 6, lines 45-46, the image pickup device comprises a CCD (14) or MOS circuit (claim 15) for reading charges from said photoelectric conversion elements in the light receiving area and transfers analog image data to said analog digital converters provided for each column (note the combination of Tran and Morris in claim 1 for parallel A/D converters for each column).

Regarding claim 16, Tran also discloses, in Fig. 1D, a shutter control unit (micro-controller 2001); and an optical system (lens 2004), and wherein said solid state image pickup device works as a digital camera (col. 6, lines 34-58).

Regarding claim 17, Tran in view of Morris further discloses positions of said photoelectric conversion elements are identified by horizontal position and vertical position (see Morris, Fig. 1 for row and column shift registers 108 & 112), and said non-volatile memory units are identified by two dimensional addresses (x, y), x and y

corresponding, respectively, to the horizontal and vertical positions of the photoelectric conversion element (see Tran, Figs. 3A-4F and col. 17, line 41 – col. 22, line 55).

Regarding claim 18, it is also seen in Tran, Fig. 1D that the micro-controller 2001 acts as horizontal address decoder which decodes horizontal address of both the photoelectric conversion elements and the non-volatile memory units since the micro-controller 2001 control all input and output operations of both the image sensor 2003 and memory 2000.

Regarding claim 19, in the combination of Tran and Morris, vertical address decoder (108 in Fig. 1 of Morris) including a scan circuit which increments the vertical address; wherein the vertical address decoder selects one of the photoelectric conversion elements rows, to send analog image data thereof to the analog-digital converters, and send converted digital image data to corresponding non-volatile memory units (note that the combined teachings of Tran and Morris provides a full control of vertical decoder and horizontal decoder to operate the parallel processing in the manner that the output signals of rows and columns from the image sensor are processed and decoded as raw/uncompressed digital image data for storing into the memory that inherently meets the claimed limitations).

4. Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tran et al. and Morris et al. as applied to claim 1 and in further view of Yamazaki et al. (US 6,556,475 B2).

Regarding claims 9 & 10, Tran and Morris are just silent about the non-volatile memory being a NAND type transistor memory (claim 9) or a NOR type transistor memory (claim 10).

However, as well recognized by Yamazaki, a non-volatile memory can be made with a NAND type transistor memory, a NOR type transistor memory, etc. (Yamazaki, col. 1, lines 40-49).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to configure the non-volatile memory in Tran with a NAND type transistor memory or an alternative NOR type transistor memory for storing image data in view of the teaching of Yamazaki because both types have a common advantage of retaining image data in memory cells even if the power supply is removed and are highly desirable for storing data in electronic devices while providing more choices and flexibility to designers for making different image pickup models based on different types of transistor memories in different camera applications.

Regarding claims 11 & 12, the combination of Tran, Morris and Yamazaki further discloses that the transistor memory has a floating gate type memory structure, MONOS type memory structure (see Yamazaki, col. 1, lines 40-49).

Regarding claim 13, the combination of Tran, Morris and Yamazaki also discloses that the transistor memory is a ferroelectric memory (see Tran, col. 4, lines 30-42).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NHAN T. TRAN
Patent Examiner